However, Applicants initially note that this section of the MPEP states that a claim which omits matter disclosed to be essential to the invention as described in the specification may be rejected under 35 USC § 112, first paragraph. However, the Examiner's Action has not rejected these claims under the first paragraph, but under the second paragraph of 35 USC § 112. Further, under the first paragraph of 35 USC § 112, such a rejection is proper only if the claim omits matter disclosed to be essential to the invention as described in the specification or in other statements of record. However, Applicants never stated within the specification or in any other statement of record that any features, which are not already cited within claim 1, are essential to the invention. The Examiner's Action has failed to provide any statement of record or description from the specification to support this rejection. Moreover, presuming that the Examiner's Action had intended to reject the claims under 35 USC § 112, second paragraph, for failing to interrelate essential elements of the invention as defined by Applicants in the specification, it is noted that Applicants never defined in the specification any elements which are essential, which are not already recited within claim 1.

It appears that the Examiner's Action maybe equating the breadth of claims 1 and 20 as being equivalent to indefiniteness. However, the MPEP §2173.04 specifically states that the breadth of a claim is not to be equated with indefiniteness. Further, there is no requirement that the exact structural cooperative relationships, as requested by the Examiner, be provided. Moreover, it is submitted that the claims are definite within the purview of 35 USC § 112, since the claims do particularly point out and distinctly claim the subject matter of the invention.

Furthermore, regarding the Examiner's assertion that the term "a majority thereof within an area defined by an outer periphery of the hole" is vague, it is noted that Applicants' specification clearly defines on page 11, lines 1-5 the intent and meaning of this term. Moreover, even viewed in a vacuum, without the benefit of the specification, it is submitted that this claim terminology is sufficiently clear to allow one skilled in the art, to whom the present invention is directed, to understand the intent and meaning of the claimed invention.

Moreover, regarding claims 6, 20 and 25, the Examiner has stated that it is not clear if the conductive layer is a signal layer, or a ground layer that is close to a signal layer. However, Applicants' claims have defined the conductive layer in conjunction with the meaning presented within Applicants' specification on page 10, lines 5-9, where it is stated that the conductive layers may include a signal ground layer 12', which serves as a ground potential for the various electronic components to be populated on the board. Thus, it is clear from Applicants' claims and specification that the signal ground layer is not a ground layer that is close to a signal layer, but is instead a ground potential.[i] It is submitted that these claims are definite within the purview of 35 USC § 112, second paragraph, and it is thus requested that this rejection be withdrawn.

The Examiner has rejected claims 1-3, 6-8, 11, 12, and 20-21 as being anticipated by *Tsukamoto* (USP 6,281,448). It is submitted that these claims are patentably distinguishable over the cited reference for at least the following reasons.

[i] It is noted that the claims do not preclude the signal ground layer from being close to another signal layer; however, this configuration is not required by the claim.

It is well settled that a reference may anticipate a claim within the purview of 35 USC § 102, only if all the features and all the relationships recited in the claim are taught by the reference structure either by clear disclosure or under the principle of inherency.

Applicants' independent claim 1 is directed to a surface laminar circuit board that includes, *inter alias*, an insulating layer, and a conductive layer disposed on an upper surface of the insulating layer. The conductive layer has a hole therein.

Tsukamoto discloses a printed circuit board which can be multi-layered circuit board as shown in Figure 5. The Figure 5 multi-layered circuit board is based on the printed circuit boards shown in Figures 1 and 2. This reference discloses that the printed circuit board shown in Figure 1 includes a base material 101 which is electrically insulative. The base material 101 has a first via hole 103 formed therein. Insulating layers 104 are provided over the base material 101. A via pad 106 is provided within the insulating layer 104. The via hole 103 is filled with conductive material which is in communication with the via pads 106. This reference further discloses forming wirings 107 in the insulating layer 104. Further, in Figure 2, it is disclosed that a further insulating layer 202 is formed over the insulating layer 104. This reference further discloses that the base material layer 101 can be made from a photo-sensitive resin.

The Examiner has interpreted the arrangement in Figure 5 in the following manner. The Examiner has equated the lower insulating layer 104 as being equivalent to Applicants' claimed insulating layer. The Examiner has equated the conductive material that fills the via holes 103 that are formed in the base material layer 101 as being a conductive layer. The Examiner has equated the base material layer 101 as

being a hole formed in the conductive layer. Further, the Examiner has equated the upper insulating layer 104 as being a dielectric layer.

However, and in contrast to the assertion presented by the Examiner's Action, this reference does not disclose (or otherwise suggest) a conductive layer that has a hole formed therein. As noted above, this reference makes clear that it is the base insulating material layer 101 that has a hole 103 formed therein. These holes 103 are then filled with a conductive material, thereby presumably forming separate islands of conductive material. These individual islands of conductive material do not constitute a conductive layer having a hole formed therein, such as would be required by Applicants' independent claim 1. It is noted that the space between adjacent ones of the filled vias does not constitute a hole within any meaning of the term, but instead simply represents a space between adjacent islands of conductive material. As such, it is submitted that the Examiner has failed to establish a *prima facie* case of anticipation against Applicants' independent claim 1.

Moreover, dependent claims 2, 3, 6-8, 11 and 12 are submitted to be patentably distinguishable over the cited reference for at least the same reasons as independent claim 1, from which these claims depend, as well as for the additional features recited therein.

Moreover, dependent claim 2 is submitted to be further patentably distinguishable over the cited reference for at least the following additionally reasons. Claim 2 recites that the dielectric layer is a photosensitive dielectric layer. The Examiner's Action asserts that the cited reference discloses that the dielectric layer is a photosensitive dielectric layer. However, the Examiner has previously equated the

dielectric layer as being the upper insulating layer 104. There is no disclosure from this reference that this upper insulating layer 104 is a photosensitive dielectric layer, as presented by the Examiner's Action. Instead, the cited reference only discloses that the base material layer 101 can be a photosensitive dielectric layer. As such, it is submitted that the Examiner's Action has failed to establish a *prima facie* case of anticipation against claim 2.

Furthermore, dependent claim 6 is submitted to be patentably distinguishable over the cited reference for at least the following additional reason. This claim recites that the conductive layer comprises a signal ground layer. The Examiner's Action has asserted that it is inherent that the conductive layer disclosed by the cited reference can be a signal layer. However, Applicants' claim does not merely recite that the conductive layer is a signal layer. Instead, Applicants' claim recites that the conductive layer is a signal ground layer, which Applicants have defined in the specification as being a layer that serves as a ground potential for the various electrical components. There is absolutely no disclosure from the reference that the material that fills the via holes 103 in the base material layer 101 serves as such a ground layer, as would be required by claim 6. As such, it is submitted that the Examiner's Action has failed to establish a *prima facie* case of anticipation against claim 6.

Furthermore, independent claim 20 is submitted to be patentably distinguishable over the cited reference in that claim 20 recites a surface laminar circuit board which includes a signal ground conductive layer. As noted above, the cited reference does not disclose a signal ground conductive layer. Moreover, claim 20 recites that the signal ground conductive layer has a hole formed therein. As argued above, the cited

reference does not disclose a conductive layer having a hole formed therein. Moreover, Applicants' claim 20 recites a photosensitive dielectric layer is disposed on an upper surface of the signal ground conductive layer. As argued above, the cited reference does not disclose such a photosensitive dielectric layer. As such, it is submitted that the Examiner's Action has failed to establish a *prima facie* case of anticipation against independent claim 20 and dependent claim 21. As such, it is requested that these claims be allowed and it is further requested that this rejection be withdrawn.

The Examiner has further rejected claims 5, 9, 10 and 23-29 as being obvious over *Tsukamoto.* It is submitted that these claims are patentably distinguishable over the cited reference for at least the following reasons.

As noted above, Applicants' independent claim 1 is *prima facie* patentably distinguishable over the cited reference. As such, dependent claims 5, 9 and 10 are submitted to be patentably distinguishable over the cited reference for at least the same reasons as independent claim 1, from which these claims depend, as well as for the additional features recite therein.

Moreover, independent claim 23 and dependent claims 24-29 are submitted to be patentably distinguishable over the cited reference for at least the following reasons.

Claim 23 is directed to a surface laminar circuit board which includes, *inter alia*, a sheet of conductive material that has a hole formed therein. The sheet of conductive material completely surrounds an area defined by the hole.

As noted above, the cited reference does not disclose or otherwise suggest a sheet of conductive material having a hole formed therein, much less a sheet of conductive material that completely surrounds an area defined by the hole. As

previously noted, the conductive material fills the via holes 103, which are formed within the base material layer 101. Thus, these filled via holes will form islands of conductive material within the base material layer 101. None of these islands of conductive material are disclosed as having a hole formed therein, which hole is surrounded by the conductive material. It is noted that the space between adjacent ones of the filled vias does not constitute a hole within any meaning of the term, but instead simply represents a space between adjacent islands of conductive material. As such, it is respectfully submitted that the Examiner's Action has failed to establish a *prima facie* case of obviousness against independent claim 23 and dependent claims 24-29. It is thus requested that these claims be allowed and that these rejections be withdrawn.

It is submitted that this application is in condition for allowance. Such action, and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,

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Date

Robert H. Berdo, Jr.
Registration No. 38,075
Customer No. 23995
(202) 659-1915 (Telephone)
(202) 659-1898 (Facsimile)

RHB:crh